REMARKS

In response to the above-identified Office Action, the Applicant submits the below remarks and respectfully requests reconsideration of the application, as amended, in light of these remarks.

The Examiner rejected claims 1-3 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,303,448 (hereinafter Chang). The Examiner rejected claim 7 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,448,094 (hereinafter Hsu). The Examiner also rejected claims 4-6 and 8-9 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent 5,567,966 (hereinafter Hwang) further in view of Hsu. The Applicant respectfully traverses this rejection for the reasons set out below.

With respect to claim 1, Chang does not teach gate electrode extending to a less shallow depth within said substrate than a depth at which the source/drain terminals are disposed. Chang teaches light doped drain (LDD) regions formed into the source/drain regions (Figure 6). The source drain regions are raised with respect to the gate electrode such that the gate electrode extends laterally beneath the top of the source/drain region (Figure 6 elements 66 and 64A; Co. 2, ll. 63-65). Thus, the Chang reference does not disclose gate electrode extending to a less shallow depth within said substrate than a depth at which the source/drain terminals are disposed.

With respect to claim 4, Hwang does not teach source/drain terminals comprising an extension, the extension extending to a more shallow depth within the substrate than the source/drain terminal to which it corresponds. This is acknowledged on page 4 of the Office Action. Hsu also does not disclose source/drain terminals comprising an extension. Hsu describes an N- doped source/drain areas that are formed adjacent to the N+ source drain areas. In Hsu N+ doped source/drain areas do not comprise the N- doped source/drain areas (Figure 2G, Column 3, ll. 52-67). Therefore, the Hsu reference also does not disclose source/drain terminals comprising an extension. As a result, the combination of the Hwang and Hsu references does not teach source/drain terminals

comprising an extension, the extension extending to a more shallow depth within the substrate than the source/drain terminal to which it corresponds.

With respect to claim 7, as described above Hsu does not teach source/drain terminals comprising an extension. In addition, the N- doped source/drain areas and N+ doped source/drain areas extend to the same depth within the substrate. Thus, Hsu does not teach source/drain terminals comprising an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds.

The Applicant submits that the rejections under 35 U.S.C. § 102(b), 102(e) and 103(a) have been addressed, and withdrawal of these rejections is respectfully requested. The Applicant furthermore submits that all pending claims are in condition for allowance, which is earnestly solicited.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicants hereby request such an extension.

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Respectfully submitted,
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MARKED UP VERSION OF THE CLAIMS

Claims 1, 4, and 7 have been amended.

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1. (Twice Amended) A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having a bottom portion and substantially vertical sidewalls;

a gate dielectric layer disposed superjacent the bottom portion of the recess and adjacent the substantially vertical sidewalls;

a gate electrode overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls, said gate electrode extending to a less shallow depth within said substrate than a depth at which the source/drain terminals are disposed; wherein the source/drain terminals [have] comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess.

4. (Twice Amended) A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having bottom portion and tapered sidewalls, the tapered sidewall surfaces forming an obtuse angle with respect to the bottom portions of the recess;

a gate dielectric layer disposed superjacent the bottom portion of the recess and adjacent the tapered sidewalls;

a gate electrode overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;

wherein the source/drain terminals [have] comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess.

7. (Twice Amended) A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having a curvilinear shape;

a gate dielectric layer disposed superjacent the curvilinear recess;

a gate electrode overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;

wherein the source/drain terminals [have] comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the curvilinear sides of the recess.